PART A: **Introduction**				
Program: **Under Graduate**		Class: **B.Sc.**	Year: **First Year**	Session: **2025-26**
Subject: **Computer Science**				
1.	Course Code			
2.	Course Title	C-1(TH): **Computer System Architecture**		
3.	Course Type (Core Course/Elective/Generic Elective/ Vocational	Core Course		
4.	Pre-Requisite (if any)	To study this course, Mathematics of 12th standard is desirable.		
5.	Course Learning Outcomes (CLO)	On completion of this course, learners will be able to: 1. Understand *(Level-2)* the basic structure, operation and characteristics of digital computer; 2. Design *(Level-6)* simple combinational digital circuits based on given parameters; 3. Understand *(Level-2)* the working of arithmetic and logic unit as well as the concept of pipelining; 4. Summarize *(Level-2)* the hierarchical memory system including cache memories and virtual memory; 5. Understand *(Level-2)* the concept and advantages of parallelism, threading, multiprocessors and multi core processors; 6. Identify *(Level-2)* the contributions Indians in the field of computer architecture and related technologies. ***Note:*** *Level of Bloom's Taxonomy is mentioned in the brackets.*		
6.	Credit Value	Theory **-4 Credits**		
7.	Total Marks	Max. Marks: **30+70**	Min. Passing Marks: **35**	
PART B: **Content of the Course**				
No. of Lectures (in hours per week): **4 Hrs. per week**				
Total No. of Lectures: **60 Hrs.**				

Module	**Topics**	**No. of Lectures**
I	Ancient Indian Contributions to Mathematics & Computation, Pingala's Binary System, Sanskrit Logic in Computing: The Nyaya and Mimamsa schools of Indian philosophy of formal logic systems. Vedic Mathematics in Computing, Vedic methods like Nikhilam Sutra and Urdhva-Tiryagbhyam Parallel Computing in Ancient Indian Architecture, comparison of stepwise computational techniques in Vedic astronomy with pipelining concepts in CPU architecture. The Sulba Sutras (ancient geometric texts) and optimized resource allocation in parallel computing models. *Fundamentals of Digital Electronics:* Data Types, Complements, Fixed-Point Representation, Floating-Point Representation, Binary and other Codes, Error Detection Codes. Logic Gates, Boolean Algebra, Map Simplification, Combinational Circuits, Sequential Circuits, simple combinational circuit design problems.	12

	Suggested activities for experiential learning: *(1) Exploring Vedic numerical techniques,* *(2) Simulating logic gates,* *(3) Verifying logic gates through truth tables.* *(3) IKS-Based Panel Discussion: Debate on how Nyaya and Mimamsa logic principles are similar to modern Boolean logic.* *(4) Research-Based Assignment: Compare Vedic mathematical techniques with modern computational algorithms.*	
II	*Circuits:* Adder, Subtractor, Multiplexer, Demultiplexer, Decoders, Encoders, Flip-Flops, Registers, Counters. *Basic Computer Organization:* Instruction codes, Computer Registers, Computer Instructions, Timing & Control, Instruction Cycles, Memory Reference Instruction, Input - Output & Interrupts, Complete Computer Description & Design of Basic Computer. Logic circuits, computer architecture, and the influence of Indian culture and history on technological advancements. ***Suggested activities for experiential learning:*** *(1) Designing combinational circuits,* *(2) Role Play: Simulate interrupt handling for I/O operations.* *(3) Circuit Design Workshop: Hands-on session on designing adders and multiplexers.* *(4) Simulation Activity: Use simulation software to design basic combinational circuits.*	08
III	*Instructions:* Instruction formats, Addressing modes, Instruction codes, Machine language, Assembly language. *Register Transfer and Micro operations:* Register Transfer Language, Register Transfer, Bus & Memory Transfer, Arithmetic Micro operations, Logic Micro-operations, Shift Micro-operations. Indian knowledge systems (such as Vedic mathematics, Sanskrit linguistic structures, and historical computing concepts) intersect with modern computational concepts like instruction formats, machine languages, and micro-operations. ancient computational methods, symbolic languages, and systems of transfer and transformation of knowledge. Panini's Ashtadhyayi and Formal Language Structure: Earliest known grammar-based rule system similar to instruction set architecture. ***Suggested activities for experiential learning:*** *(1) Categorize instructions into different formats and know the relationship between opcodes, operands, and addressing modes,* *(2) Understand how processors access operands in memory,* *(3) Comparative Analysis: Students explore Panini's rule-based grammar and compare it with modern instruction set design.* *(4) Coding Exercise: Simulate a simple CPU instruction execution using a high-level programming language.*	10
IV	*Processor and Control Unit*: Hardwired vs. Micro programmed, Control Unit, General Register Organization, Stack Organization, Instruction Format, Data Transfer & Manipulation, Program Control, Introductory concept of RISC, CISC, advantages and disadvantages of both. Pipelining: Concept of pipelining, introduction to pipelined data path and control Handling, Data hazards & Control hazards.	10

	Suggested activities for experiential learning: *(1) Presentation on CPU pipeline execution.* *(2) Hardware vs. Microprogrammed Control Debate: Pros and cons of both techniques.* *(3) Build Your Own CPU Model: Group project designing a simplified processor.* *(4) Case Study on Modern CPUs: Analyze how modern processors handle instruction execution.*	
V	*I/O Systems and Memory:* Peripheral Devices, I/O Interface, Data Transfer Schemes - Program Control, Interrupt, DMA Transfer, I/O Processor. Memory Hierarchy, Processor vs. Memory Speed, High-Speed Memories, Main memory, Auxiliary memory, Cache Memory, Associative Memory, Interleaving, Virtual Memory, Memory Management. Ancient Manuscript Storage (Nalanda, Takshashila Libraries): Similarity to hierarchical memory and indexing methods. *Vedic Indexing and Categorization:* Conceptually linked to associative and cache memory. ***Suggested activities for experiential learning:*** *(1) Research Assignment: Compare manuscript storage methods with modern hierarchical memory.* *(2) Cache Memory Simulation: Hands-on activity to understand cache memory replacement policies.* *(3) Field Visit (if possible): Visit a digital archive/library to understand memory organization.* *(4) Hands-on with Virtual Memory: Implement paging in an OS.*	10
VI	*Parallelism:* Meaning, types of parallelism, introduction to Instruction level-parallelism, Parallel processing challenges, Applications. *Flynn's classification:* Introduction to SISD, SIMD, MISD, MIMD Hardware *Multithreading:* Introduction, types, advantages and applications. *Multicore processors*: Introduction, advantages, difference from multiprocessor. *Parallel Computation in Indian Astronomy:* Aryabhata and Bhaskara II's models of planetary motion involve computations similar to parallel processing. ***Suggested activities for experiential learning:*** *(1) Case study and quiz based on parallel processing,* *(2) Presentation on CPU pipeline execution* *(3) Comparative Analysis: Explore ancient Indian parallel calculations vs. modern parallel processing.* *(4) Multithreading Workshop: Implement parallelism using OpenMP or CUDA.* *(5) Mini-Project: Implement matrix multiplication using multithreading.*	8

VII	Indian contributions: Contributions of reputed scientists of Indian origin – Dr. Vinod Dham — Father of Intel Pentium Processor, Dr. Ajay Bhat — Co-Inventor of USB Technology, Dr. Vinod Khosla —Cofounder of Sun Microsystems, Dr. Vijay P Bhatkar —Architect of India's national initiative in supercomputing, and many others. Parallel Computing projects of India — PARAM, ANUPAM, FLOSOLVER, CHIPPS etc., other relevant contributors and contributions. ***Suggested activities for experiential learning:*** *(1) Research on Indian contributions to computing,* *(2) Research on supercomputers in India* *(3) Documentary Screening: Films on India's supercomputing projects.* *(4) Expert Talk: Invite an Indian computing expert for a guest lecture.* *(5) Group Research Project: Prepare case studies on Indian innovators in computing.* *(6) Coding Competition: Solve real-world problems inspired by PARAM's computational models.*	2

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PART C: **Learning Resources**
Textbooks, Reference Books, Other Resources

Suggested Readings:

- M.Morris Mano, "Computer System Architecture", PHI.
- William Stalling, "Computer Organization & Architecture", Pearson Education Asia.
- V. Carl Hamacher, "Computer Organization", TMH
- Tannenbaum, "Structured Computer Organization", PHI.
- Vedic Mathematics by Bharati Krishna Tirtha
- Shukla, K. S. (1976). Aryabhata and His Work.
- Joseph, G. G. (1991). The Crest of the Peacock: Non-European Roots of Mathematics.
- Pingree, D. (1978). Mathematical Astronomy in India.
- Staal, F. (2006). The Science of Language and Logic in India.
- Kiparsky, P. (2009). Panini as a Formalist.
- Cardona, G. (1976). Panini: A Survey of Research.
- Balasubramaniam, R. (2009). Knowledge Management in Ancient India.
- Rajaraman, V. (2009). Computers and Information Technology.
- Bhatkar, V. (2016). Supercomputing in India.
- Narasimhan, R. (1990). India's IT Revolution.

Suggestive digital platform web links:

https://epgp.inflibnet.ac.in/Home/ViewSubject?catid=fBYckQKJvP3a/8Vd3L08tQ==

https://epgp.inflibnet.ac.in/Home/ViewSubject?catid=uUIVj2W71X+8mppiIHe0+A==

https://www.yout-ube.com/watch?v=4TzMyXmzL8M

https://nptel.ac.in/courses/1 06/106/ 106106166/

https://nptel.ac.in/courses/1 06/106/ 106106134/

Suggested equivalent online courses:

https://nptel.ac.in/courses/106/1 05/ 106105163/

Part D: Assessment and Evaluation		
Suggested Continuous Evaluation Methods: Maximum Marks: **100** Continuous Comprehensive Evaluation (CCE): **30** Marks University Exam (UE): **70** Marks		
Internal Assessment: Continuous Comprehensive Evaluation (CCE)	Class Test Assignment/Presentation	**Total Marks: 30**
External Assessment: University Exam (UE) Time: 03.00 Hours	Section (A): Objective type Section (B): Short Questions Section (C): Long Questions	**Total Marks: 70**

PART A: **Introduction**			
Program: **Under Graduate**	Class: **B.Sc.**	Year: **First Year**	Session: **2025-26**
Subject: **Computer Science**			

1.	Course Code		
2.	Course Title	C-1(PR): **Computer System Architecture (Lab)**	
3.	Course Type (Core Course/Elective/Generic Elective/Vocational	Core Course	
4.	Pre-Requisite (if any)	To study this course, Mathematics of 12thstandard is desirable.	
5.	Course Learning Outcomes (CLO)	On completion of this course, learners will be able to: 1. Describe *(Level-1)* the basic logic and universal gates; 2. Classify *(Level-2)* the behavior of logic gates using truth tables; 3. Implement *(Level-3)* Binary-to -Gray, Gray-to -Binary code conversions; 4. Design *(Level-6)* half and full adder circuit using basic gates; 5. Design *(Level-6)* and construct flip flops and verify the excitation tables. ***Note:*** *Level of Bloom's Taxonomy is mentioned in the brackets.*	
6.	Credit Value	Practical - **2 Credits**	
7.	Total Marks	Max. Marks: **100**	Min. Passing Marks: **35**

PART B: **Content of the Course**

No. of Lab. Practical (in hours per week): **2 Hrs. per week**

Total No. of Labs: **60 Hrs.**

	Suggestive list of Practical	No. of Labs.
	1. To study basic gates (AND, OR, NOT) and verify their truth tables. 2. To convert a given binary number to Gray code using IC 7486. 3. To study and verify NAND as Universal gate using IC 7400. 4. To study half adder using basic gates and verify its truth table. 5. To study Full Adder using basic gates and verify its truth table. 6. To realize basic gates (AND, OR, NOT) from Universal gates (NAND and NOR). 7. To verify truth table of 4-bit adder using IC 7483. 8. To design and construct RS flip Flop using gates and verify the truth table. 9. To design and construct JK flip Flop using gates and verify the truth table. 10. To verify De-Morgan's Theorem.	

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Suggested equivalent online courses: https://nptel.ac.in/courses/106/105/106105163/

PART D: Assessment and Evaluation

Suggested Continuous Evaluation Methods:

Internal Assessment	**Marks**	**External Assessment**	**Marks**
Class Interaction/Quiz	**NIL**	Viva Voce on Practical (20 marks)	**100**
Attendance		Practical Record File (20 marks)	
Assignments (Charts/Model/Seminars / Technology Dissemination/ Excursion/ Lab visit/ Industrial Visit)		Table Work / Exercise Assigned (60 marks)	
	Total Marks: 100		

Prof. Navita Shrivastava
Chairman Board of Studies